 10724963 update

POWER SAVING METHODS FOR PROGRAMMABLE LOGIC ARRAYS

This Application is a Continuation-in-Part Application (CIP) of a co-pending Patent Application 10/187,515 filed on July 2, 2002, which is a U.S. Patent 6,658,638. Patent Application 10/187,515 claims a Priority Date of September 27, 2001 of a Patent Application filed in United States Patent and Trademark Office with a serial number 09/966,141 (Docket number SHAU-9802C) filed on September 27, 2001 by the Applicant of this Application now U. S Patent 6,492,835. Patent 6,492,835 is a continuation of application Ser. No. 09/005,113, filed Jan. 9, 1998, now U.S. Pat. No. 6,314,549.

FIELD OF THE INVENTION

The present invention relates to circuit design methods for programmable logic arrays, and more particularly to power saving methods for programmable logic arrays.

BACKGROUND OF THE INVENTION

Programmable logic array (PLA) circuits and gate array (GA) logic circuits are the most common building modules for integrated circuit (IC) logic products. After IC designers describe logic operations by hardware description language (HDL), computer aid design (CAD) tools automatically translate the HDL into PLA or gate array circuits. These two methods (PLA or GA) are exchangeable. Most of logic circuits can be implemented by either way. PLA CAD tools combine all the logic relationships between a large number of input and output signals into one large group of AND operations followed by one large group of OR operations, and represent those operations by arrays of programmable connections. The physical structure of a PLA is highly regular, and its timing is easily predictable. On the contrary, gate array CAD tools break down complex logic calculations into series of single step logic operations such as NAND, NOR, INVERT, and implement those logic operations by a large number of logic gates. Such procedure is called "synthesizing" in the art. The physical structures of GA logic circuits are nearly random. That is why they are often called "random logic circuits" in the art. It usually requires very complex connections between logic gates. As IC fabrication technologies progressed into deep sub-micron, the resistance of conductor lines and the coupling capacitors between conductors became significant. The complex connections in GA logic circuits make timing